Claims 1 and 4

Applicant respectfully submits that the cited references fail to teach or suggest that "each of the master IC and the at least one slave IC has an input terminal for receiving the **display control signal** output from the **display control signal generation section of the master IC** through an external wiring," as required by claims 1 and 4.[1/] The Examiner concedes that Bird et al. fail to teach of suggest "a master IC and at least one slave IC." The Examiner cites Strobel et al. as teaching these missing recitations. However, as shown in FIG. 5 of the Strobel et al. reference, Applicant submits that neither the master nor the slave has an input terminal for receiving the display control signal output from the display control signal generation section of the master IC through an external wiring."

The signals that are input into terminals C1, C2 shown in FIGS. 4A and 5 of Strobel et al. are not output from a "**display control signal** generation section" in the master IC, as required by claims 1 and 4, but are instead inputs to the master driver and slave driver via the bus that is connected to terminals provided between VLCD and GND terminals.

Moreover, there is nothing shown in FIGS. 4A and 5 of Strobel et al. that suggests a "display control signal generation section" provided in the master IC, as required by claims 1 and 4. Moreover, neither of the terminals C1, C2 shown in FIGS. 4A and 5 of Strobel et al. are for receiving a "**display control signal** based on a signal from an external MPU," as required by claims 1 and 4. Rather, as discussed at col. 12, lines 35-37 of Strobel, "terminals C1 and C2 ...permit the

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1/ Exemplary benefits associated with some embodiments of the present invention are discussed, for example, at p. 3, lines 26 - p. 4, lines 14 and p. 19, line 16 – p. 20, line 19 of the present application.

operating mode of the IC to be selected." As discussed at col. 13, lines 57-60 of Strobel, "operating modes can be selected via the inputs C1 and C2 and specifically, by means of the operating mode control BAS and by means of logical elements or multiplexers which correspond to the switches S1 and S2 shown in FIG. 3." (Emphasis added.) The signals input at C1 and C2 are not used to control the display, and therefore are not "display control" signals, as claimed. [2]

Thus, Applicant respectfully submits that the cited references fail to teach or suggest at least the above recitations of claim 1. Accordingly, Applicant respectfully submits that claim 1 is patentable over the cited references. In addition, Applicant respectfully submits that dependent claims 2 and 3 are patentable at least by virtue of their dependency from independent claim 1. Applicant further submits that independent claim 4 is patentable for at least the same reasons, and that dependent claims 16 and 17 are patentable at least by virtue of their dependency from independent claim 4.

Claims 2 and 16

Applicant respectfully submits that the cited references fail to teach or suggest that each of the master IC and the at least one slave comprises "a driver which supplies a data signal based on the display data read out from the display memory to the first electrodes," or that "the display control signal input through the input terminal is supplied to the display address circuit and the driver," as required by claims 2 and 16.

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[2] / As noted at page 11, lines 22-26 of the present application, "the display control signals are needed in view of the operations of the display address circuit 118 and the driver 120. As examples of the display control signals, a latch pulse LP, reset signal RES, gray scale control pulse GCP, and polar-inversion signal FR shown in Figure 4 can be given."

The Examiner concedes that Bird et al. fail to teach of suggest "a master IC and at least one slave IC." The Examiner cites col. 5, lines 9-56 of Strobel et al. as teaching these missing recitations. However, as shown in FIG. 4a of the Strobel et al. reference, there is nothing in Strobel et al. that indicates that "the display control signal input through the input terminal is supplied to the display address circuit and the driver," as required by claims 2 and 16. As discussed at col. 12, lines 35-37 of Strobel, "terminals C1 and C2 ...permit the operating mode of the IC to be selected." However, Applicant respectfully submits that there is **nothing** in Strobel et al. that would suggest that the signals input at **C1, C2 are supplied to the display address circuit and the driver**. Applicant notes that "the driver" recited in claims 2 and 16 is different than the first and second drivers recited in claims 1 and 4.

Thus, Applicant respectfully submits that the cited references fail to teach or suggest at least the above recitations of claims 2 and 16. Accordingly, Applicant respectfully submits that claims 2 and 16 are patentable over the cited references.

Claims 3 and 17

Applicant respectfully submits that the cited references fail to teach or suggest the display control signal generated in the display control signal generation section "includes a gray scale control pulse for generating the pulse width modulation signal."

The Examiner concedes that Bird et al. fail to teach of suggest "a master IC and at least one slave IC." Nevertheless, the Examiner cites Bird et al. as teaching that the display control signal "includes a gray scale control pulse for generating the pulse width modulation signal," as required by claims 3 and 17. If Bird et al. fails to teach a master IC, then it follows that Bird et al. fails to teach a display control signal generation section since the claims require that the display control signal

generation section is part of the master IC. Because the display control signal generation section generates the display control signal, Bird et al. could not teach a display control signal since Bird et al. does not teach a display control signal generation section. Thus, Bird et al. could not possibly teach that the display control signal "includes a gray scale control pulse for generating the pulse width modulation signal," as required by claims 3 and 17.

Applicant therefore respectfully submits that the cited references fail to teach or suggest at least the above recitations of claims 3 and 17. Accordingly, Applicant respectfully submits that claims 3 and 17 are patentable over the cited references.

Claims 5 and 7

Applicant respectfully submits that the cited references fail to teach or suggest a master IC comprising "an internal delay circuit which delays the display control signal."

The Examiner concedes that Bird et al. fail to teach or suggest "a master IC and at least one slave IC," or "an internal delay circuit." The Examiner cites Strobel et al. as teaching these missing recitations, and in rejecting claims 5 and 7, takes the position that "Strobel et al. teach an internal delay circuit through terminals C1 and C2, and thus is variable."

However, as shown in FIG. 4a of the Strobel et al. reference, there is nothing in Strobel et al. that indicates that the master includes an internal delay circuit "which delays the display control signal," and "an output terminal which outputs the display control signal before the display control signal passes through the internal delay circuit," as required by claims 5 and 7. The Examiner asserts that the display control signal is input at terminals C1, C2. In the event the Examiner seeks to maintain this ground of rejection, Applicant respectfully requests that the Examiner cite a specific portion of the reference that supports this position

Applicant further respectfully submits, for at least the reasons described above with respect to claims 1 and 4, that the cited references fail to teach or suggest that there is also nothing shown in FIGS. 4A and 5 of Strobel et al. that suggests a "display control signal generation section" provided in the master IC, as required by claims 5 and 7. Moreover, neither of the terminals C1, C2 shown in FIGS. 4A and 5 of Strobel et al. are for receiving a "**display control signal based on a signal from an external MPU**," as required by claims 5 and 7.

Thus, Applicant respectfully submits that the cited references fail to teach or suggest at least the above recitations of claim 5. Accordingly, Applicant respectfully submits that claim 5 is patentable over the cited references. In addition, Applicant respectfully submits that dependent claim 6 is patentable at least by virtue of its dependency from independent claim 5. Applicant further submits that independent claim 7 is patentable for at least the same reasons, and that new dependent claim 18 is patentable at least by virtue of its dependency from independent claim 7.

Claims 8-15

In rejecting claims 8 and 12, the Examiner concedes that the SMOS reference fails to teach or suggest that "the display control signal generation section is enabled and the display control signal is output from the output terminal when the display driver IC is set as a master by the selection terminal" or that "the display control signal generation section is disabled when the display driver IC is set as a slave by the selection terminal," as required by claims 8 and 12. The Examiner cites Strobel et al. as supplying these missing limitations.

Applicant respectfully submits that the Official Action has shown no motivation to combine the cited references, and further that absent impermissible hindsight reconstruction, there would be no motivation to combine the references.

Applicant also respectfully submits that the Strobel et al. reference also fails to teach or suggest that "the display control signal generation section is enabled and the display control signal is output from the output terminal when the display driver IC is set as a master by the selection terminal" or that "the display control signal generation section is disabled when the display driver IC is set as a slave by the selection terminal," as required by claims 8 and 12.

Rather, as noted above, the Strobel et al. reference simply fails to disclose a "display control signal generation section." As such, Applicant submits that the Strobel et al. reference also fails to suggest that "the display control signal generation section is enabled and the display control signal is output from the output terminal when the display driver IC is set as a master by the selection terminal" or that "the display control signal generation section is disabled when the display driver IC is set as a slave by the selection terminal," as required by claims 8 and 12. The Strobel et al. reference simply fails to disclose enabling or disabling of a "display control signal generation section."

Thus, Applicant respectfully submits that the cited references fail to teach or suggest at least the above recitations of claims 8 and 12. Accordingly, Applicant respectfully submits that claims 8 and 12 are patentable over the cited references. In addition, Applicant respectfully submits that dependent claims 9-11 and 13-15 are patentable at least by virtue of their dependency from independent claims 8 and 12, respectively.

Claim 12

In addition to the reasons discussed above, Applicant respectfully submits that the cited references also fail to teach or suggest that "the display control signal generation section is enabled, and the display control signal generated in the display control signal generation section is output through the output terminal and

input to the internal delay circuit, when the display driver IC is set as a master by the selection terminal," as required by claim 12. In addition, Applicant respectfully submits that the cited references fail to teach or suggest "an internal delay circuit which delays the display control signal generated in the display control signal-generating circuit," as required by claim 12. Applicant further respectfully submits that the cited references also fail to teach or suggest "a signal selection circuit for selecting the transition state of the logic of one of the display control signal input through the internal delay circuit and the display control signal input through the input terminal," as required by claim 12.

Thus, Applicant respectfully submits that the cited references also fail to teach or suggest at least the above recitations of claim 12. Accordingly, Applicant respectfully submits that claim 12 is patentable over the cited references for at least this additional reason.

The art made of record but not relied upon by the Examiner has been considered. However, it is submitted that this art neither describes nor suggests the presently claimed invention.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6793 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: May 22, 2003

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